What is claimed is:

1. A random access memory, comprising:

a first memory bank;

a second memory bank;

an error checking circuit operatively connected to receive data read from the first memory bank; and

a multiplexer operatively connected to input data read from both the first memory bank and the second memory bank, wherein input selection of the multiplexer is controlled by an output of the error checking circuit.

2. The random access memory of claim 1, wherein the first memory bank and second memory bank comprise static random access memory.

3. The random access memory of claim 1, wherein the error checking circuit comprises a parity checking circuit.

4. The random access memory of claim 1, wherein when the parity checking circuit determines parity of the data read from the first memory bank is correct, the multiplexer selects the input from the first memory bank, and when the parity checking circuit determines parity of the data read from the first memory bank is incorrect, the multiplexer selects the input from the second memory bank.

5. The random access memory of claim 1, wherein the first memory bank, the second memory bank, the error checking circuit, and the multiplexer are implemented on a single chip.

6. The random access memory of claim 1, further comprising means for writing data simultaneously to the first memory bank and the second memory bank.

7. A partitioned memory system, comprising:

a first memory device;

a second memory device;

means for writing data to the first and second memory devices in parallel;

means for error checking data read from the first memory device and outputting a result indicative thereof; and

selection means for selecting data read from the first memory device for output to a bus if the result from the error checking means indicates no error and for selecting data read from the second memory device for output to the bus if the result from the error checking means indicates an error.

8. The memory system of claim 7, wherein the first memory device and the second memory device comprise static random access memory.

9. The memory system of claim 7, wherein the error checking means comprises means for checking parity.

10. The memory system of claim 7, wherein the selection means comprises a multiplexer.

11. The memory system of claim 7, wherein the first memory device, the second memory device, the error checking means, and the selection means are implemented on a single chip.

12. A method for reducing errors in a memory system, comprising:

writing data into first and second memory banks of the memory system in parallel;

reading data from a desired location of the first memory bank;

checking the data read from the first memory bank for errors;

if no errors are present, outputting the data read from the first memory bank to a bus; and

if the data read from the first memory bank contains errors, outputting data read from a parallel location in the second memory bank to the bus.

13. The method to claim 12, wherein checking the data read from the first memory bank for errors comprises checking the data for parity

14. The method of claim 12, wherein the data read from the first memory bank is cleared for parity on a byte-by-byte basis.

15. The method of claim 12, wherein data from one of the first memory bank and second memory bank are selected using a multiplexer.

16. A partitioned static random access memory comprising:

a first static random access memory bank;

a second static random access memory bank, the first and second static random access memory banks being configured such that data may be written to parallel locations therein;

a parity checking circuit configured to check parity of data read from the first static random access memory bank and to output a result indicative thereof; and

a multiplexer configured to receive data read from the parallel locations in the first and second static random access memory banks and to select one of said data depending upon the result output by the parity checking circuit.